FPGA IP CORE

HIGH-SPEED DATA INTERFACE FOR SIMERA SENSE XSCAPE IMAGERS

OVERVIEW

The Zaitra XSCAPE Readout IP Core is a lightweight, high-performance FPGA IP Core developed by Zaitra for direct integration with Simera Sense xScape imagers. It captures and converts high-speed image data streams into usable formats, enabling rapid deployment in satellite and edge processing systems.

Designed for compatibility with AMD Zynq™ UltraScale+™ and Zynq™ 7000 SoCs, it delivers efficient, real-time data processing using a single AXI4-Stream-based IP core.

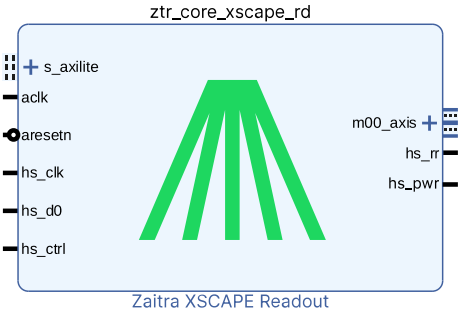
Key Features

PLUG-AND-PLAY INTEGRATION

- Fully compatible with all xScape imagers
- Works with AMD Zynq™ UltraScale+™ MPSoC and Zynq™ 7000 SoC
- Ready-to-use CLI application for fast deployment

HIGH-SPEED DATA HANDLING

- Compatible with all imager data readout configurations up to 400Mbps.
- Supports SDR and DDR mode.
- Packet parsing and image formatting in real time
- CRC-32 data integrity verification with automatic packet rejection and error status reporting for corrupted packets



STANDARDS-COMPLIANT ARCHITECTURE

- AXI4-Lite and AXI4-Stream interface
- Verified with standard Xilinx AXI DMA IP Core

VERSATILE OPERATION MODES

- Bypass Mode – Outputs raw packets
- RAWL Mode – Outputs binary raw image (little endian)
- TIFF Mode – Outputs uncompressed TIFF with metadata

SOFTWARE INTEGRATION

- Supplied with CLI, a Python-based control tool
- Automates readout, band sequencing, metadata parsing
- Full support for multi-band sensors with user-space control

FPGA RESOURCE UTILIZATION

Resource	Value
LUTs	1087
Flip-Flops	1770
BRAM	13
DSP	1

Zaitra s.r.o, Bauerova 491/10,
603 00 Brno, Czech republic